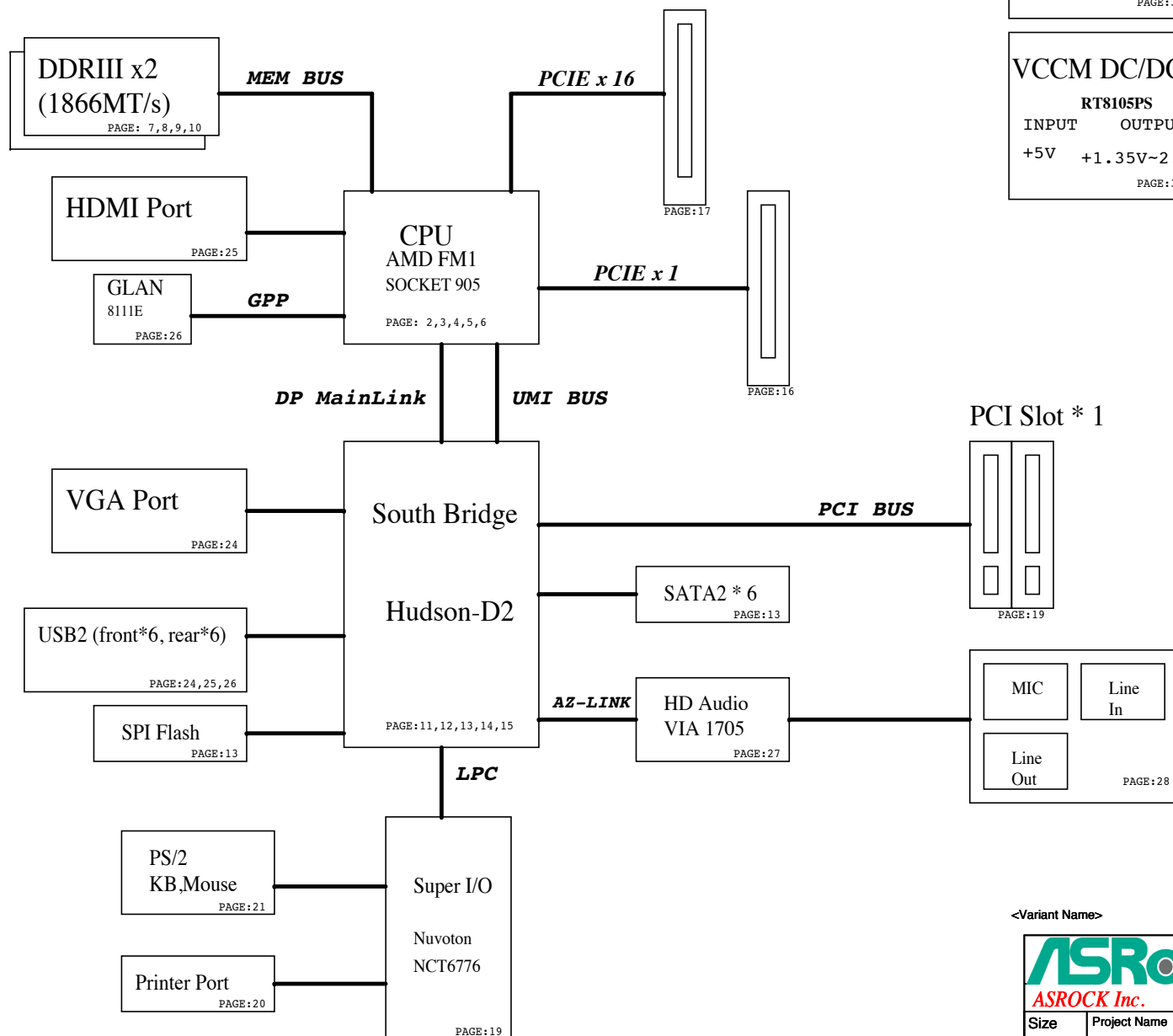


# A55M-HVS

Revision: G/A 1.03

AMD FM1 + Hudson-D2 uATX



## 1.2V DC/DC

APW7120	
INPUT	OUTPUT
+3V	+1.1V~1.8V

PAGE: 33

## ATX Power

INPUT	OUTPUT
+5VSB	+12V
+3.3V	-5V
+5V	-12V

PAGE: 29

## VCCM DC/DC

RT8105PS	
INPUT	OUTPUT
+5V	+1.35V~2.0V

PAGE: 32

## CPU DC/DC

L6717	
INPUT	OUTPUT
+12V	+1.1V~2.0V

PAGE: 34, 35

## System Regulator

INPUT	OUTPUT
+5VSB	+3VSB
+3VSB	+1.1VSB
+3V	+2.5V
VCCM	VTT_DDR
VCCM	+1.1VSB

PAGE: 30

## PCB LAYER

L1 : Component (S1)  
L2 : VCC  
L3 : GND  
L4 : Solder (S4)

**CAD Note:**  
Default Resistor and Capacitor footprint is SMD 0402 type. Different resistor footprints are showed on schematics.

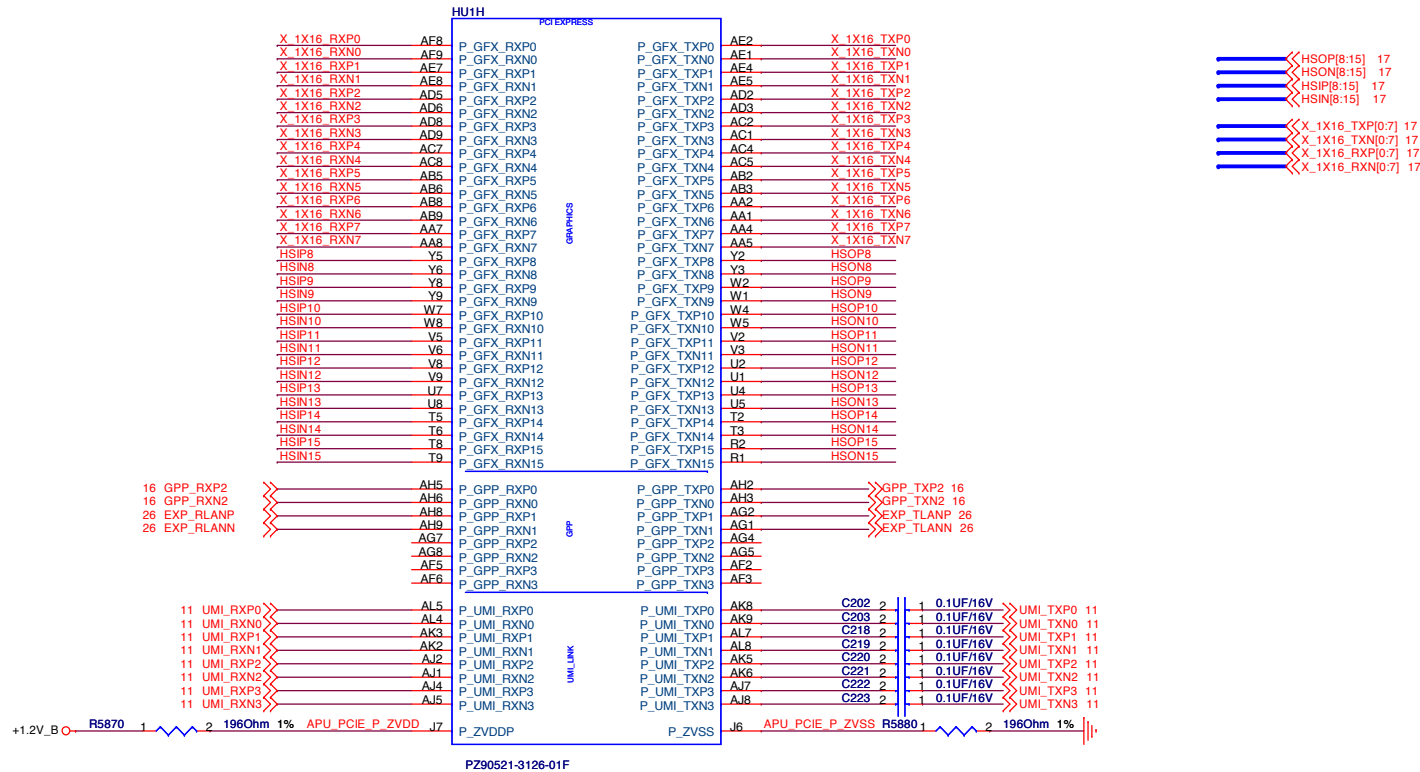
/ = Not Installed Part

<Variant Name>

<b>ASRock</b> Title : <b>BLOCK</b>	
ASROCK Inc. Engineer: <b>Mingus_Wu</b>	
Size	Project Name
Custom	<b>A55M-HVS</b>
Date: Friday, July 22, 2011	Rev 1.03
Sheet 1	of 39

www.vinafix.vn

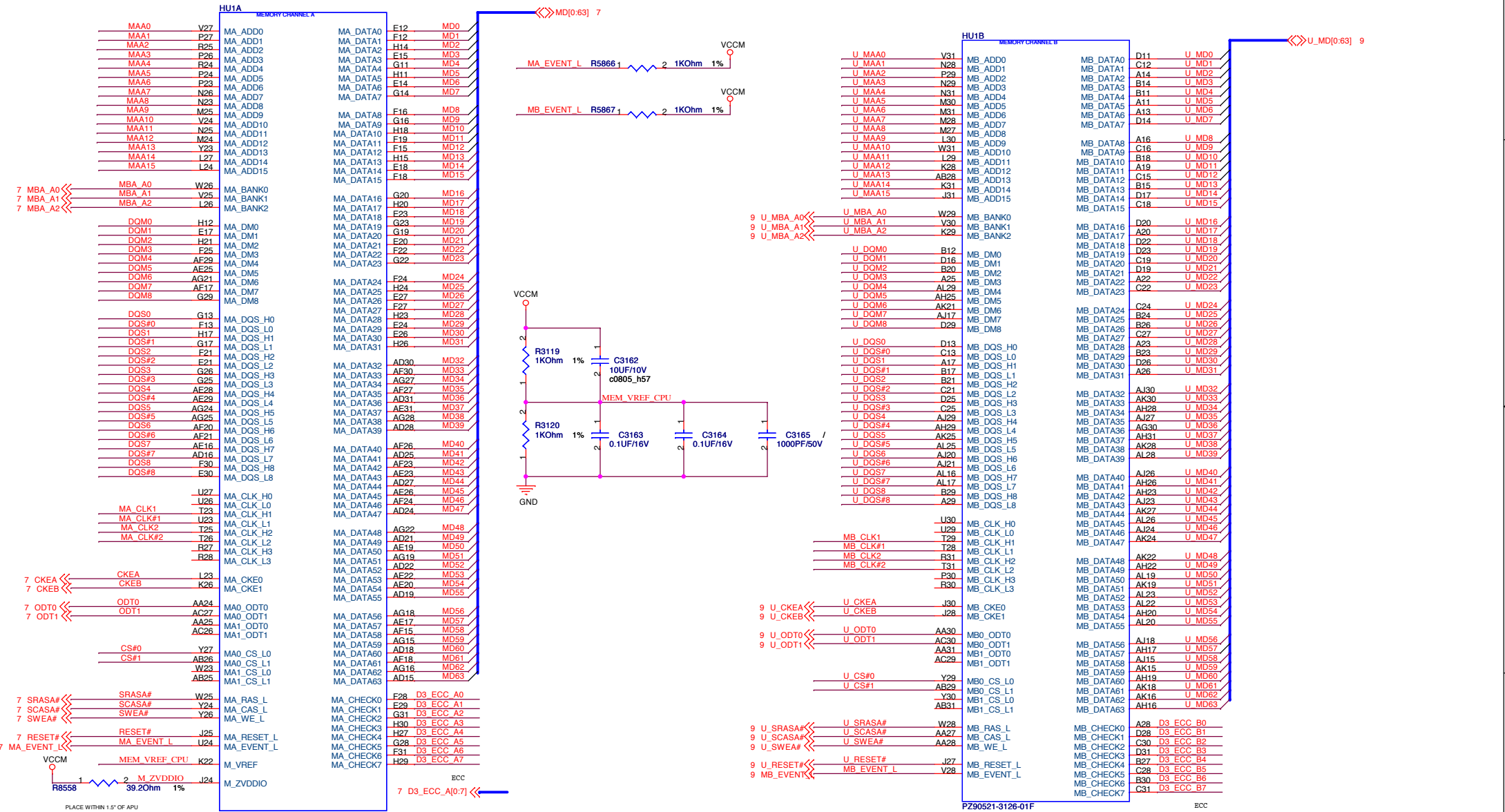
# CPU HyperTransport Interface



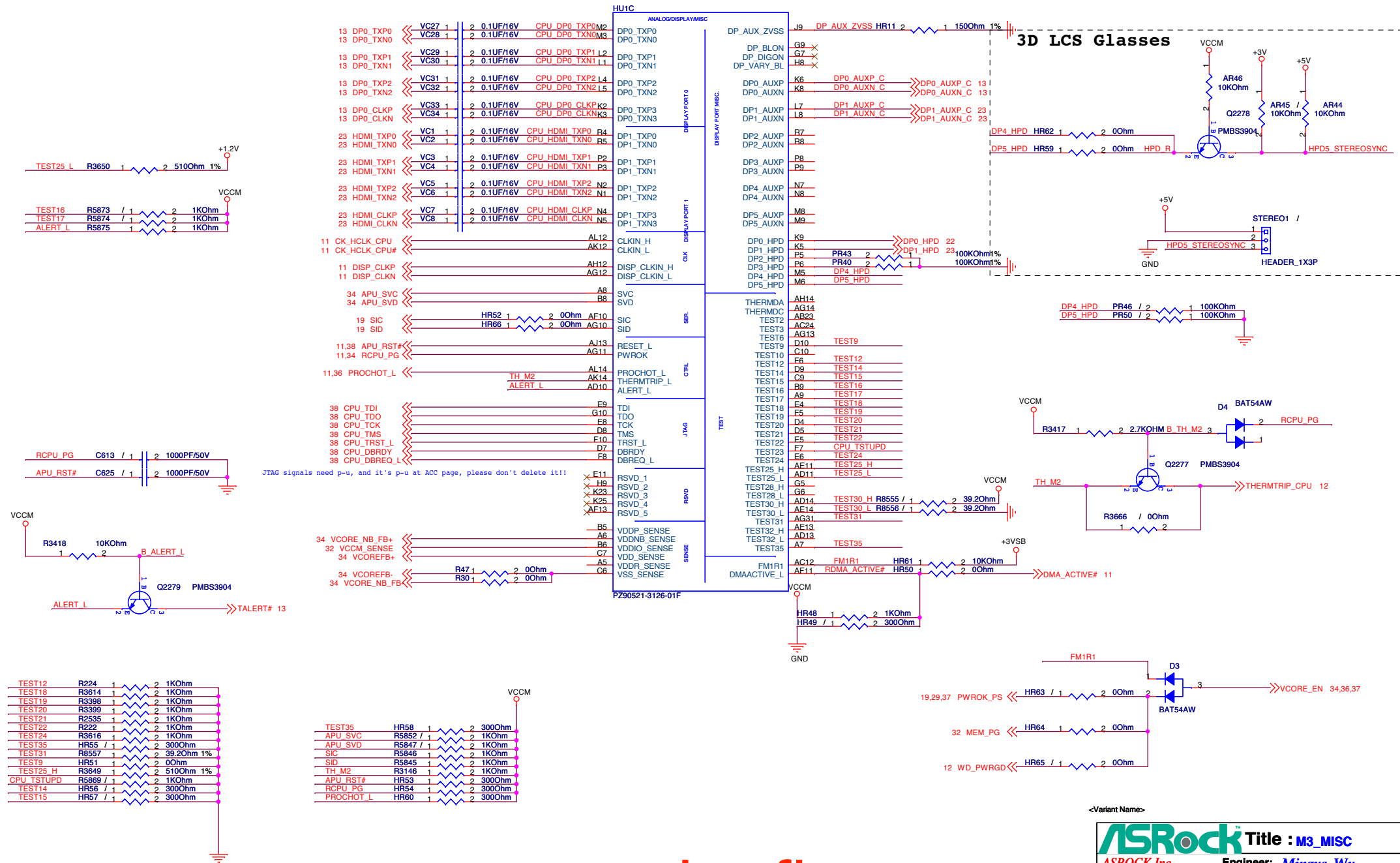
<Variant Name>

<b>ASRock</b> Title : M3_HDT		Engineer: <i>Mingus_Wu</i>	
Size A3	Project Name <b>A55M-HVS</b>		Rev 1.03
Date: Friday, July 22, 2011		Sheet 2	of 39

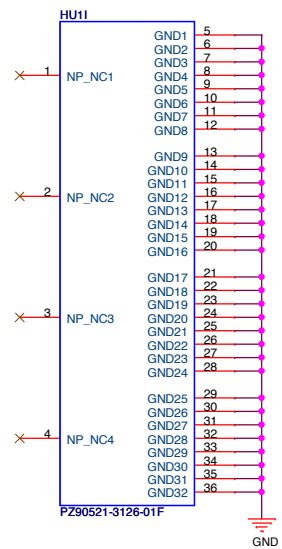
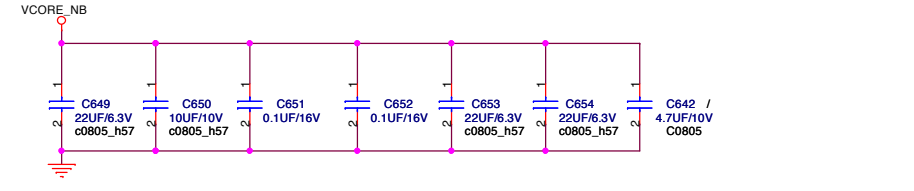
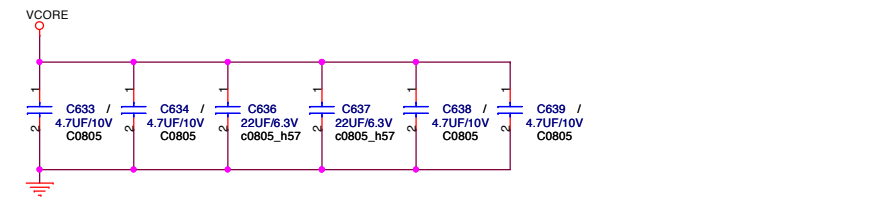
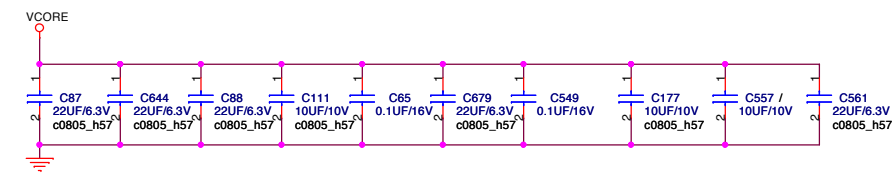
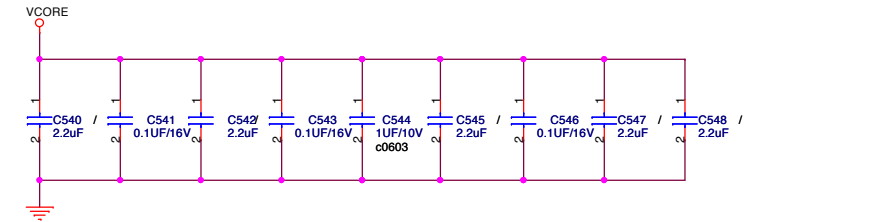
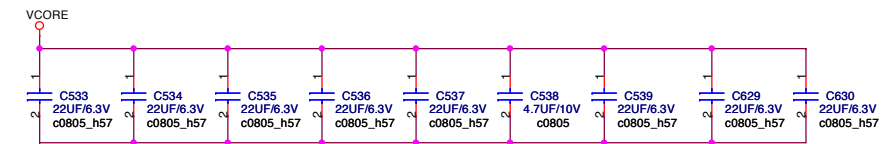
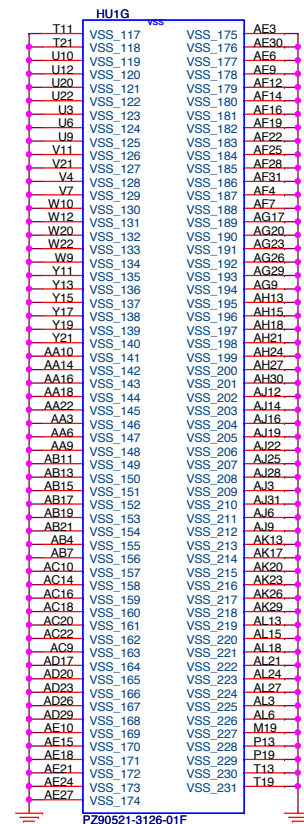
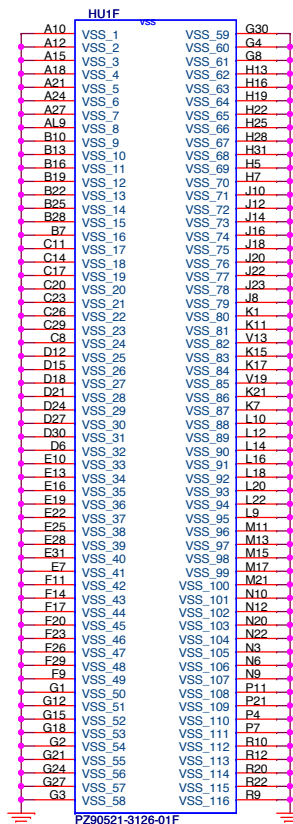
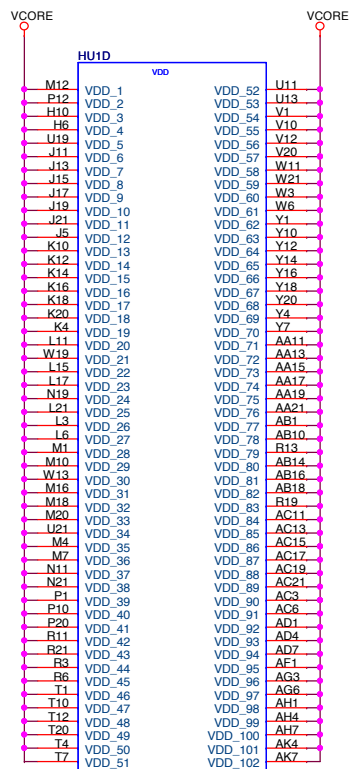
# CPU DDR3 Memory Interface



## CPU Control & Debug Interfaces




# Processor Power & Ground





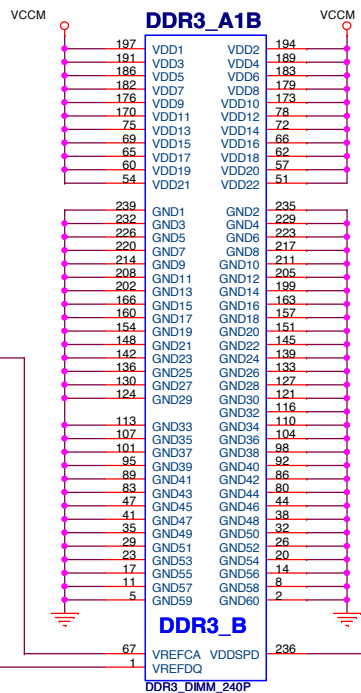
DDR3 A1A



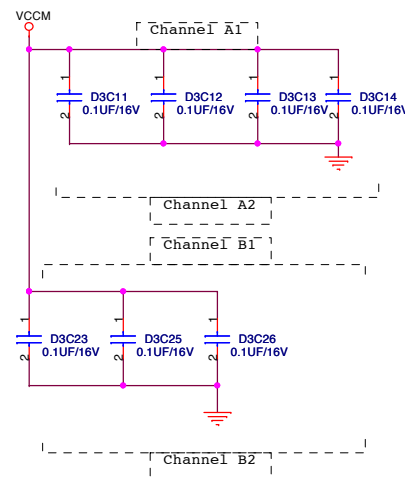
		<b>Title :</b> DDRIII_DIMM1&3	
<b>ASRock Inc.</b>		<b>Engineer:</b> <i>Mingus_Wu</i>	
<b>Size</b> A3	<b>Project Name</b>  <div style="font-size: 1.5em; font-weight: bold; color: blue;">A55M-HVS</div>	<b>Rev</b> 1.03	
<b>Date:</b> Friday, July 22, 2011		<b>Sheet</b> 7	<b>of</b> 39

10 D3\_VREFDQ  
10 D3\_VREFCA

If you don't use  
MEM\_WARN, please  
connect PIN116 and  
PIN 239 to GND.



If you don't use  
MEM\_WARN, please  
connect PIN2 and  
PIN121 to GND.

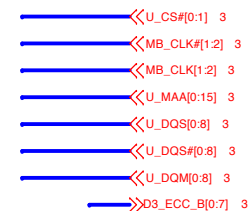
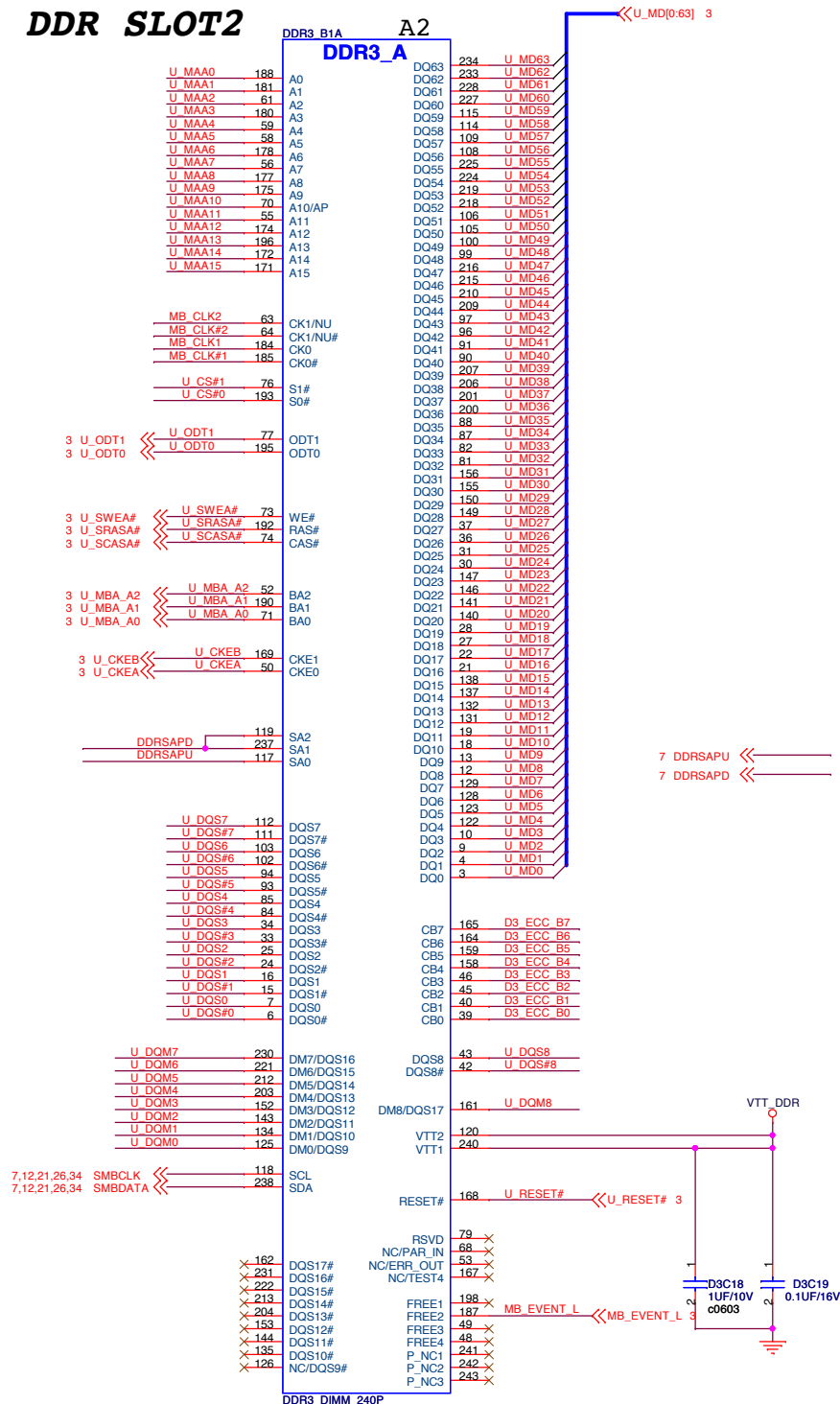


With AMT    W/O AMT  
+3V\_CL    +3V  
S0~S5有電    S0有電

<Variant Name>

ASRock		Title : DDR3L_POWER_L0	
ASROCK Inc.		Engineer: Mingus_Wu	
Size A3	Project Name A55M-HVS	Rev 1.03	
Date: Friday, July 22, 2011		Sheet 8	of 39



**DDR SLOT2**

<Variant Name>

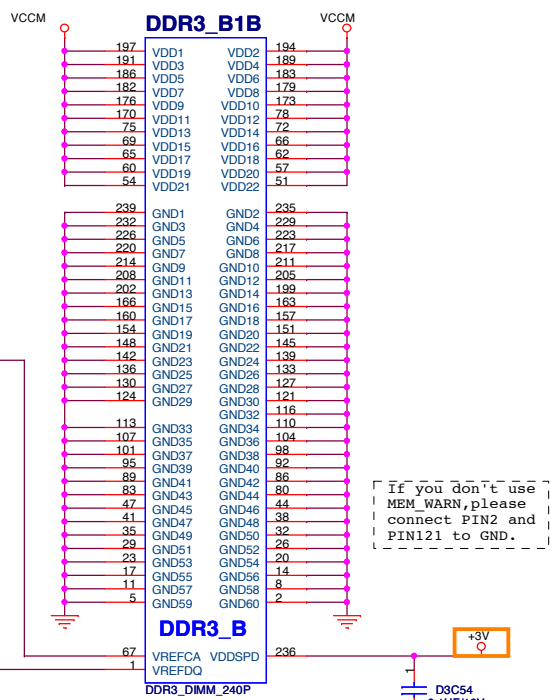
		<b>Title :</b> DDRIII_DIMM2&4	
<b>ASRock Inc.</b>		<b>Engineer:</b> <i>Mingus_Wu</i>	
<b>Size</b> A3	<b>Project Name</b>  <div style="font-size: 1.5em; font-weight: bold;">A55M-HVS</div>	<b>Rev</b> 1.0	
<b>Date:</b> Friday, July 22, 2011		<b>Sheet</b> 9	<b>of</b> 39

8 D3\_VREFDQ  
8 D3\_VREFCA

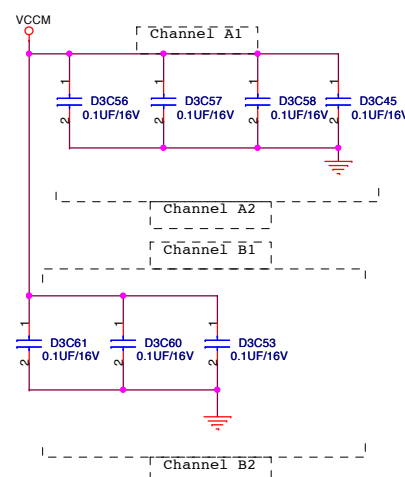
If you don't use MEM\_WARN, please connect PIN116 and PIN 239 to GND.



If you don't use MEM\_WARN, please connect PIN116 and PIN 239 to GND.



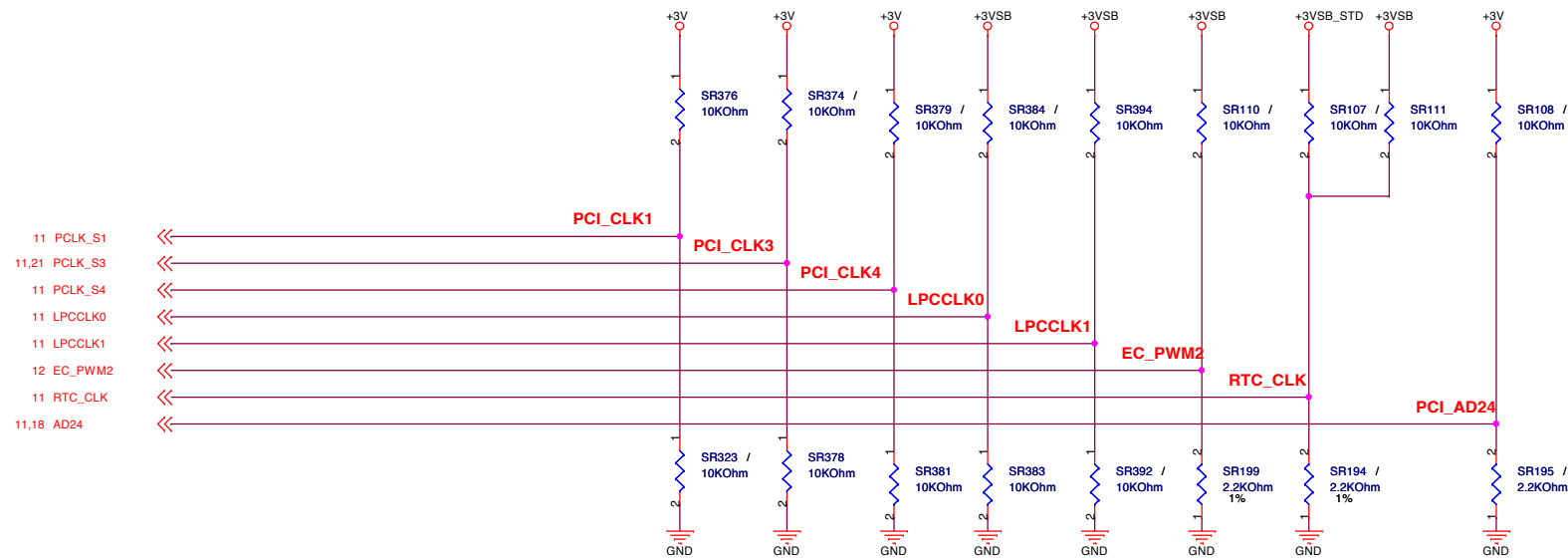
If you don't use MEM\_WARN, please connect PIN2 and PIN121 to GND.



With AMT W/O AMT  
+3V CL +3V  
S0-S5有電 S0有電

<Variant Name>

ASRock		Title : DDRIII_POWER_H	
ASROCK Inc.		Engineer: Mingus Wu	
Size A3	Project Name A55M-HVS	Rev 1.03	
Date: Friday, July 22, 2011		Sheet 10	of 39

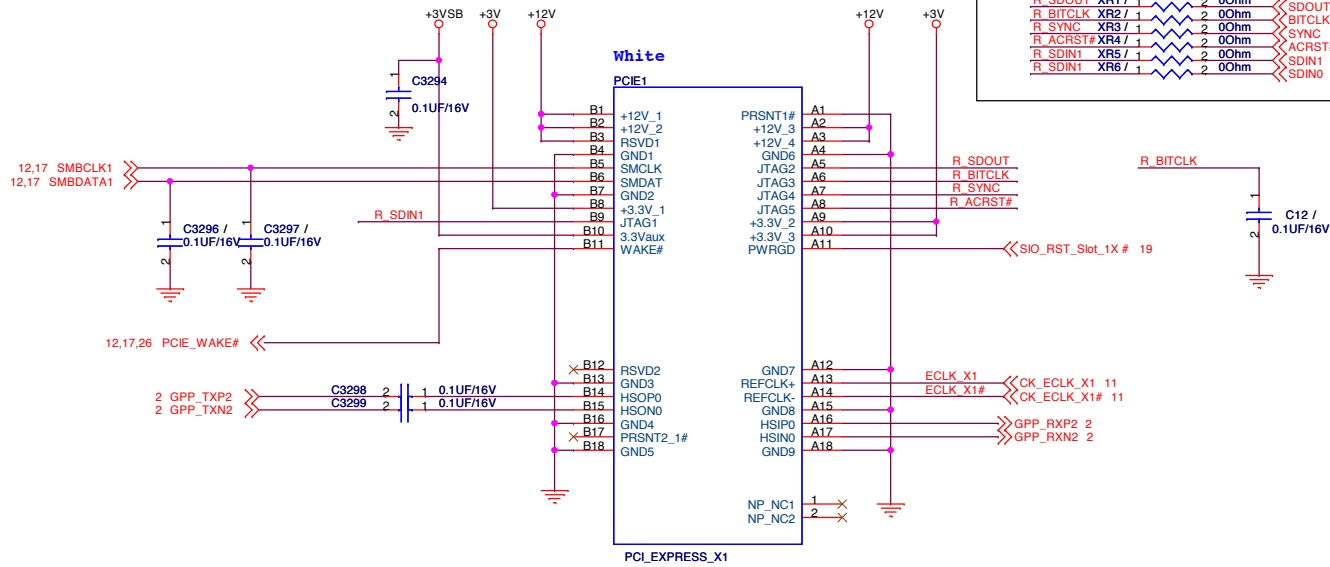


## REQUIRED STRAPS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPCCLK0	LPCCLK1	RTC_CLK	EC_PWM2	PCI_AD24
<b>PULL HIGH</b>	Allow PCIe Gen2 DEFAULT	Enabled Debug straps	NON-FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	S5+ DISABLE DEFAULT	ROM TYPE: H = LPC ROM	Default PCIe straps
<b>PULL LOW</b>	Force PCIe Gen1	Disabled Debug straps DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	S5+ ENABLE	L = SPI ROM DEFAULT	EEPROM PCIe straps DEFAULT

Reserved Creative Malcolm sound card

R\_SDOUT\_XR1 / 1 2 00hm SDOUT 12,27  
R\_BITCLK\_XR2 / 1 2 00hm BITCLK 12,27  
R\_SYNC\_XR3 / 1 2 00hm SYNC 12,27  
R\_ACRST#\_XR4 / 1 2 00hm ACRST# 12,27  
R\_SDIN1\_XR5 / 1 2 00hm SDIN1 12  
R\_SDIN1\_XR6 / 1 2 00hm SDIN0 12,27

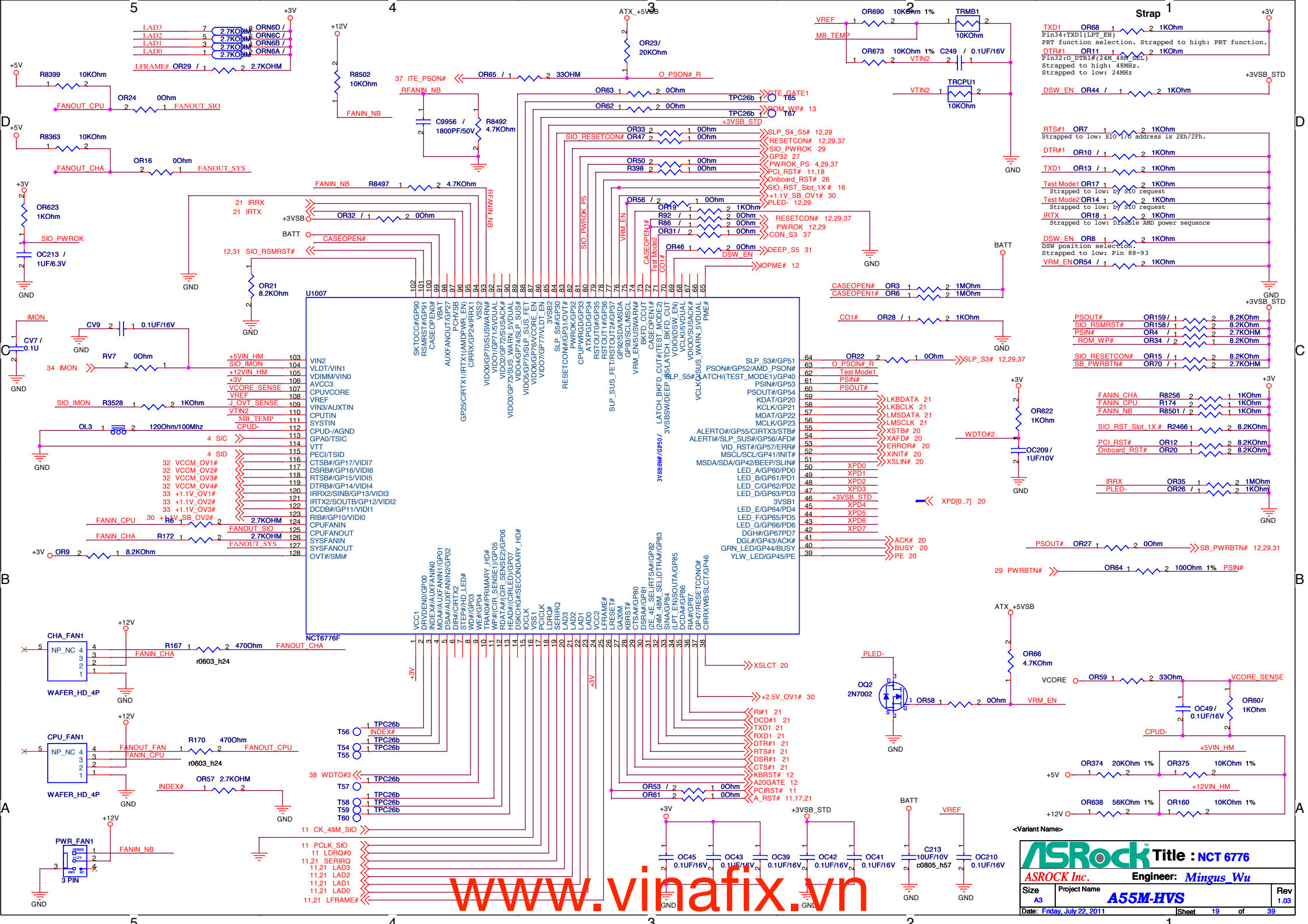


<Variant Name>

<b>ASRock</b> ™		Title : PCIE_X1 SLOT	
ASROCK Inc.		Engineer: Mingus_Wu	
Size A3	Project Name <b>A55M-HVS</b>		Rev 1.03
Date: Friday, July 22, 2011		Sheet 16	of 39

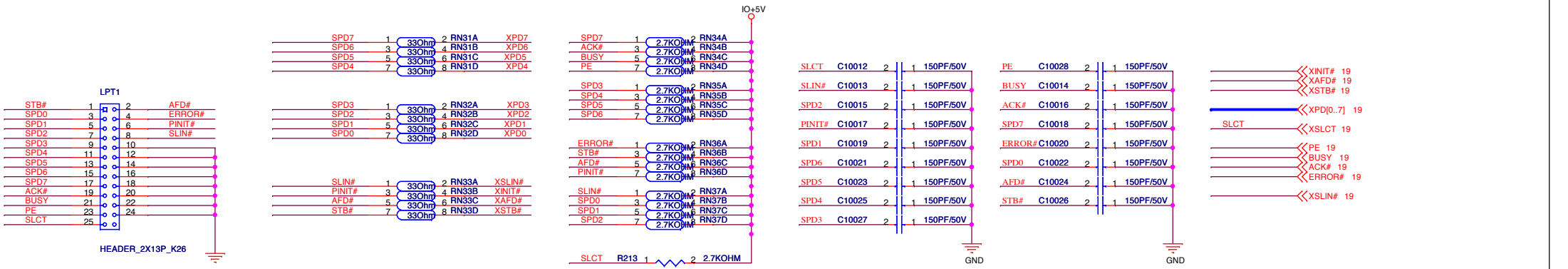


[www.vinafix.vn](http://www.vinafix.vn)

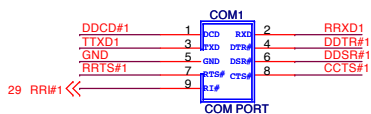


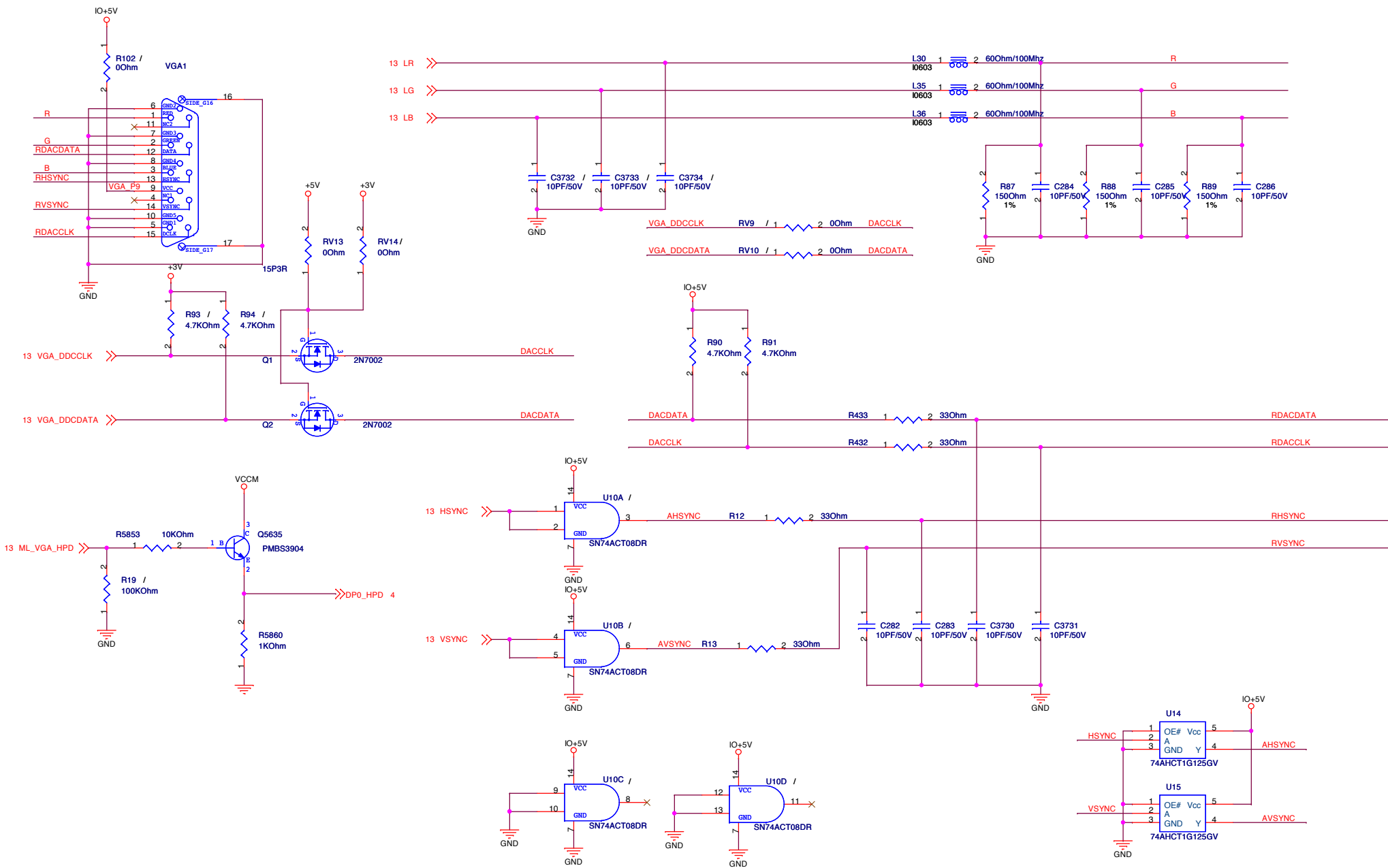
www.vinafix.vn

Parallel Port



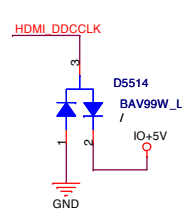
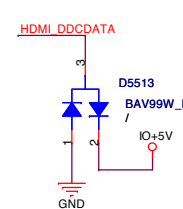
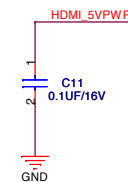
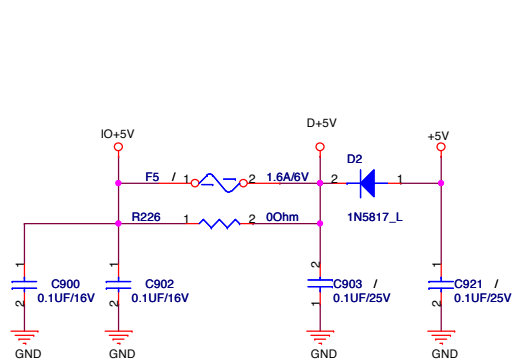
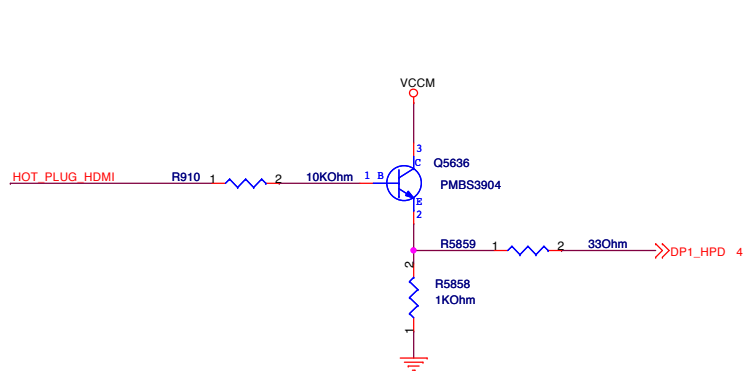
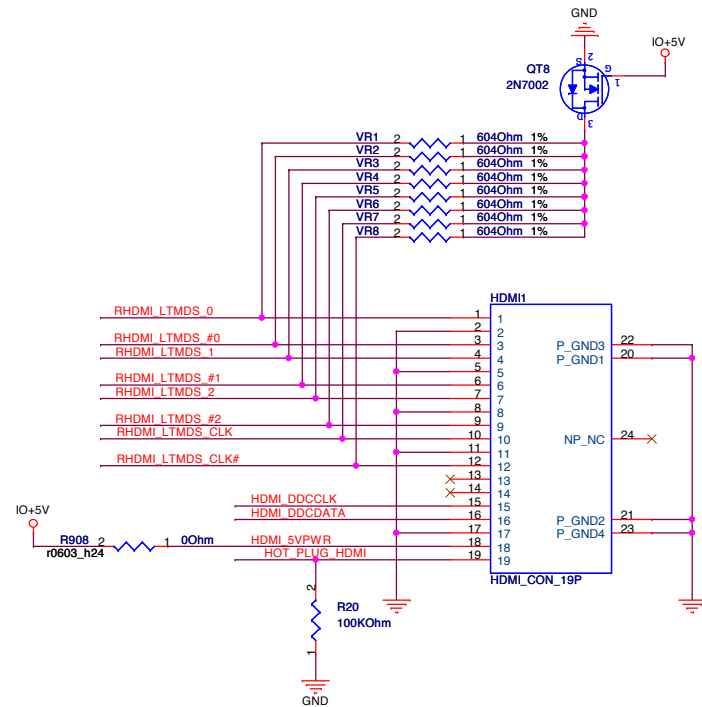
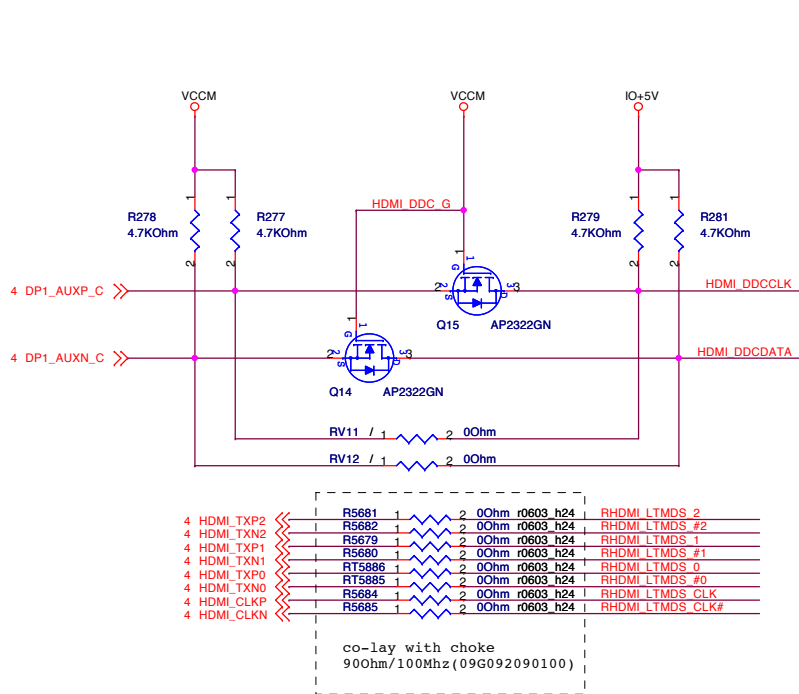






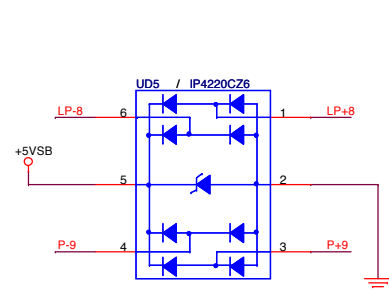
<Variant Name>

# HDMI

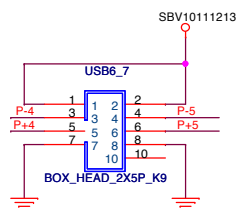


<Variant Name>

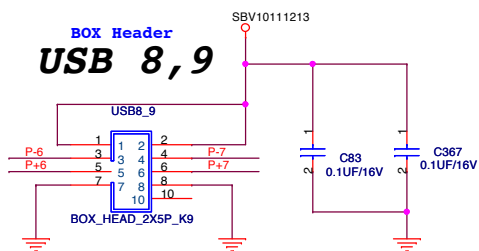
ASRock		Title : HDMI	
ASROCK Inc.		Engineer: Mingus_Wu	
Size A3	Project Name	A55M-HVS	
Date: Friday, July 22, 2011	Sheet	23	of 39
		Rev	1.03



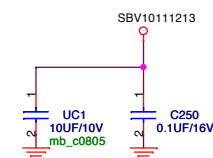
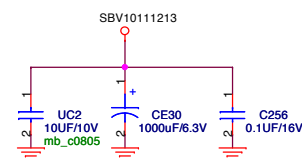
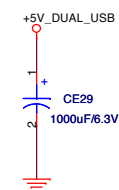
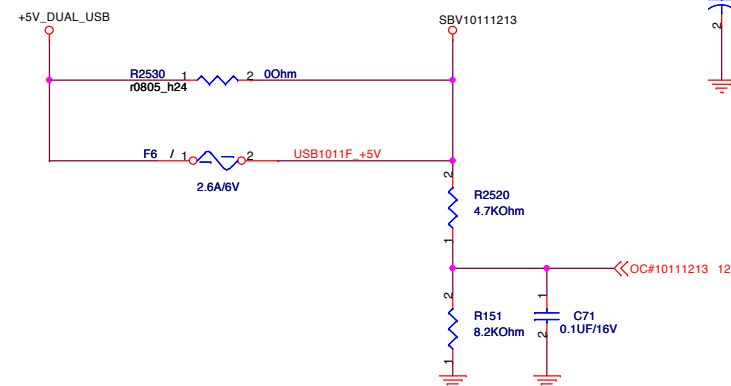
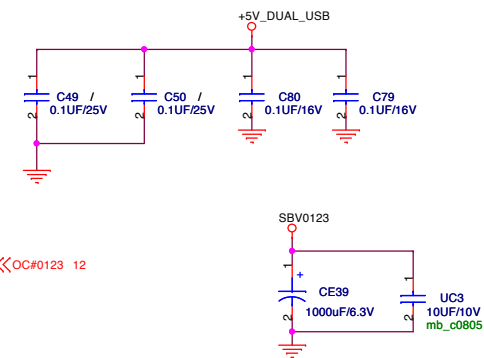
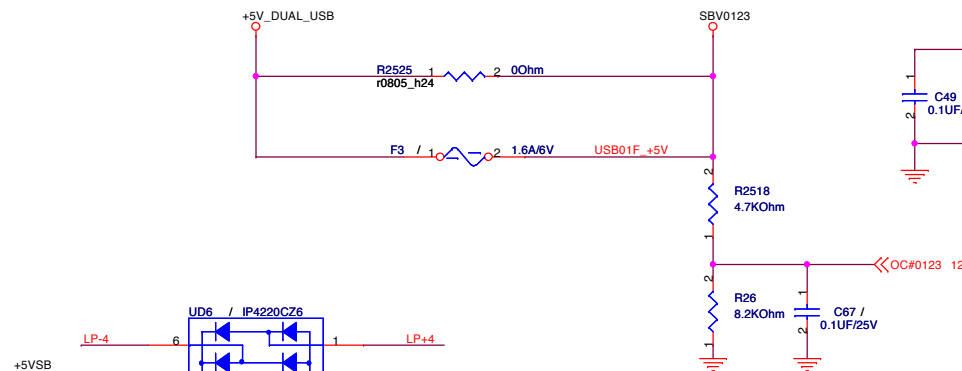
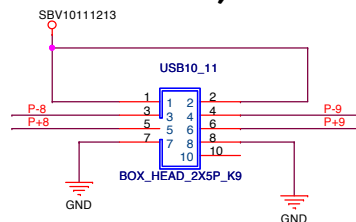
BOX Header  
**USB 6,7**



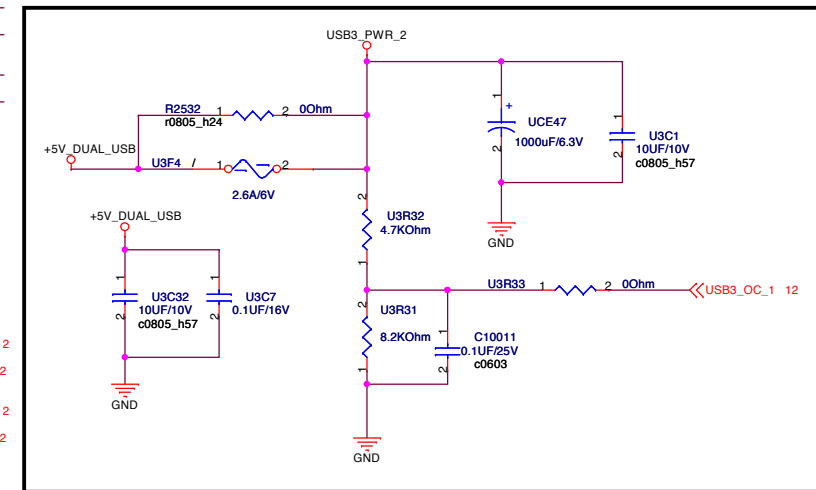
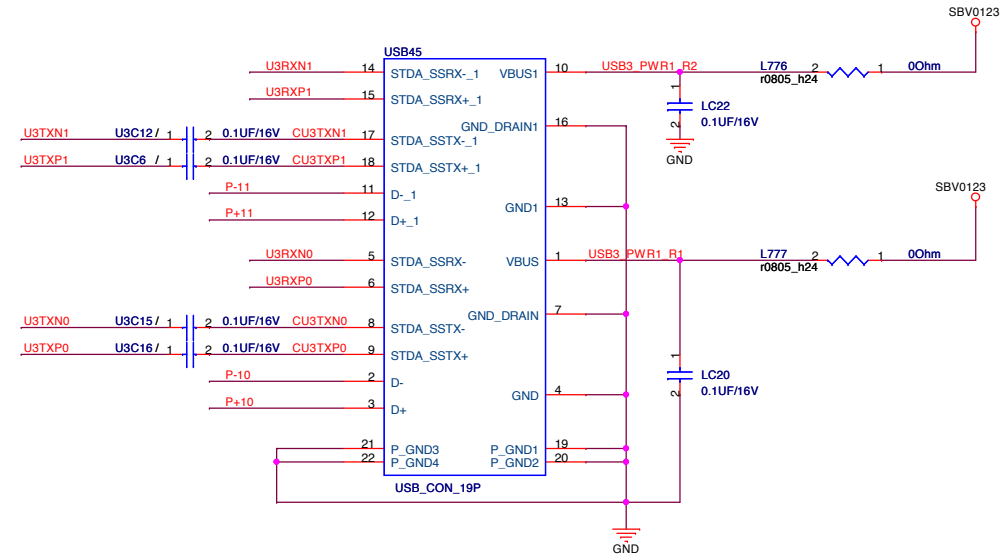
BOX Header  
**USB 8,9**



**BOX Header**  
***USB10,11***



		<b>Title :</b> USB_PORT	
<b>ASRock Inc.</b>		<b>Engineer:</b> Mingus_Wu	
<b>Size</b> A3	<b>Project Name</b> A55M-HVS	<b>Rev</b> 1.03	
<b>Date:</b> Friday, July 22, 2011		<b>Sheet</b> 24 <b>of</b> 39	

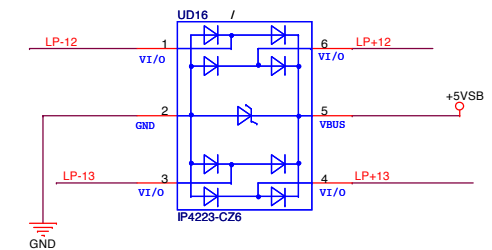
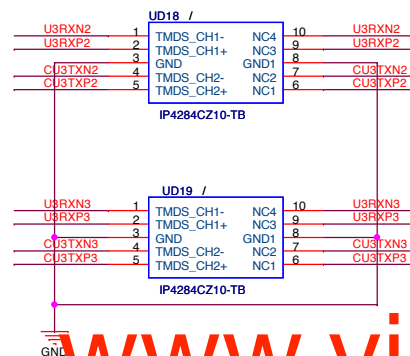


12 LP-13    << >>    P-13

12 LP+13    << >>    P+13

12 LP-12    << >>    P-12

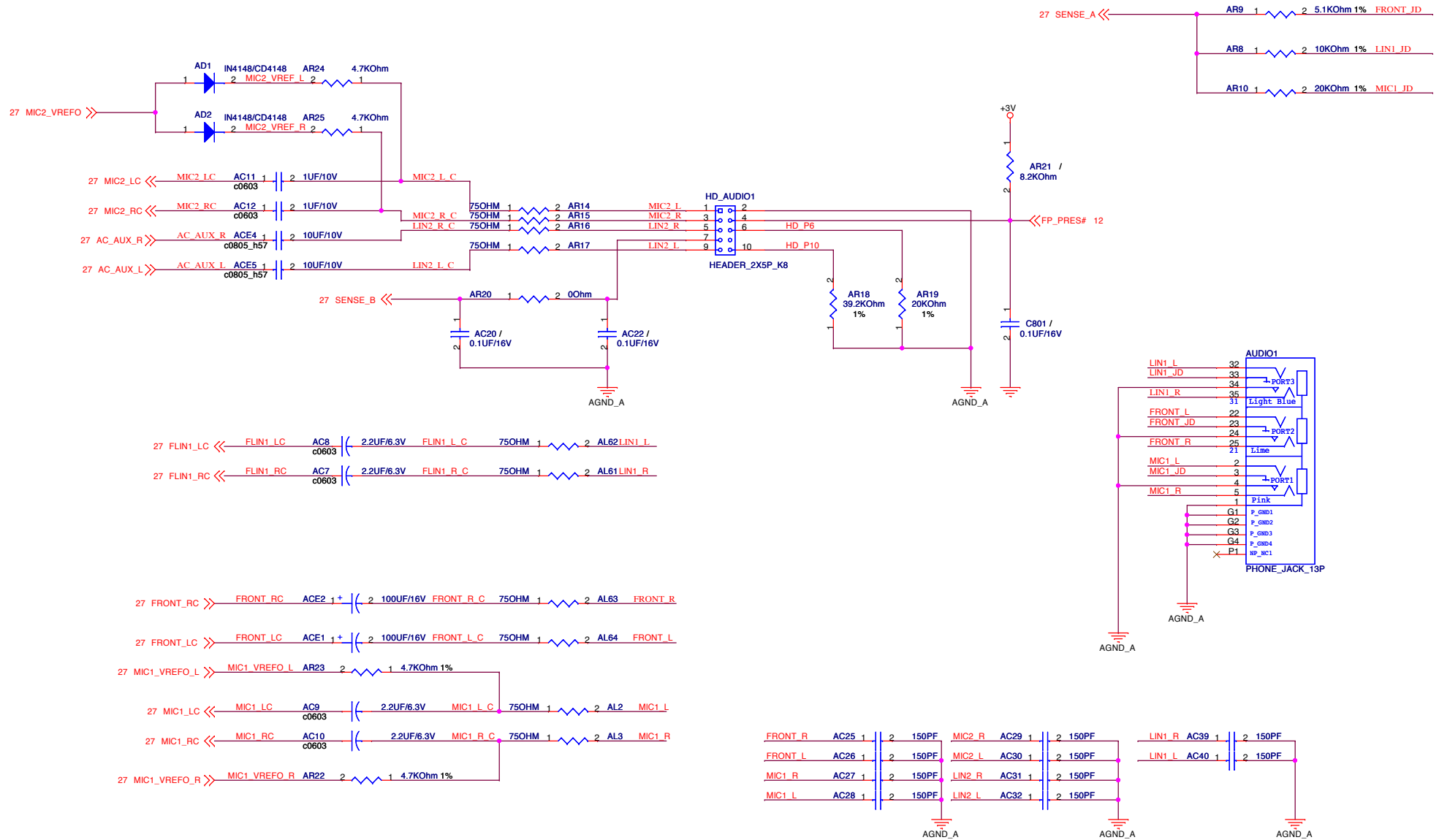
12 LP+12    << >>    P+12



		<b>Title :</b> U3 RIO	
<b>ASRock Inc.</b>		<b>Engineer:</b> <u>Mingus_Wu</u>	
<b>Size</b> A3	<b>Project Name</b>  <div style="font-size: 1.5em; font-weight: bold;">A55M-HVS</div>	<b>Rev</b> 1.03	
<b>Date:</b> Friday, July 22, 2011		<b>Sheet</b> 25 <b>of</b> 39	





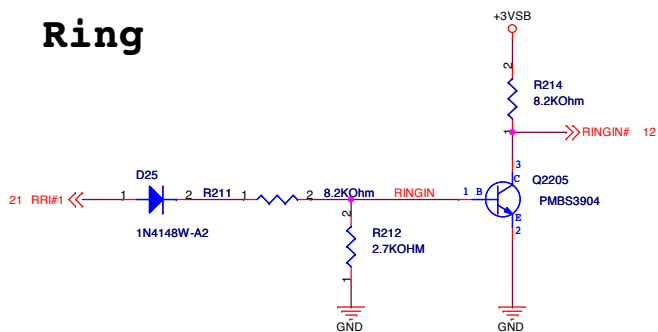


<Variant Name>

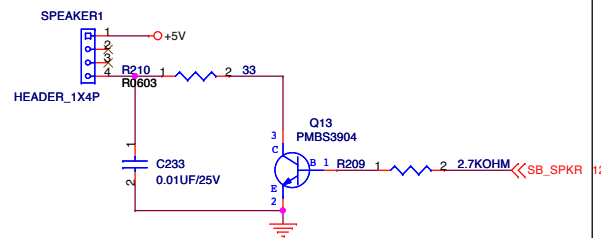
<b>ASRock</b> ™		<b>Title : AUDIO CONN</b>	
ASROCK Inc.		Engineer: <i>Mingus_Wu</i>	
Size A3	Project Name <b>A55M-HVS</b>	Rev 1.03	
Date: Friday, July 22, 2011	Sheet 26	of 39	



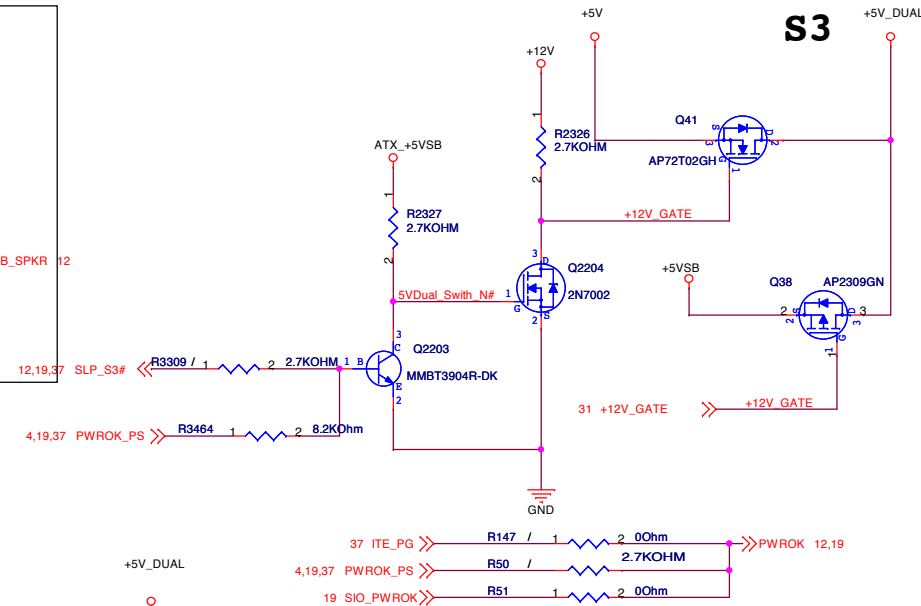
## Ring



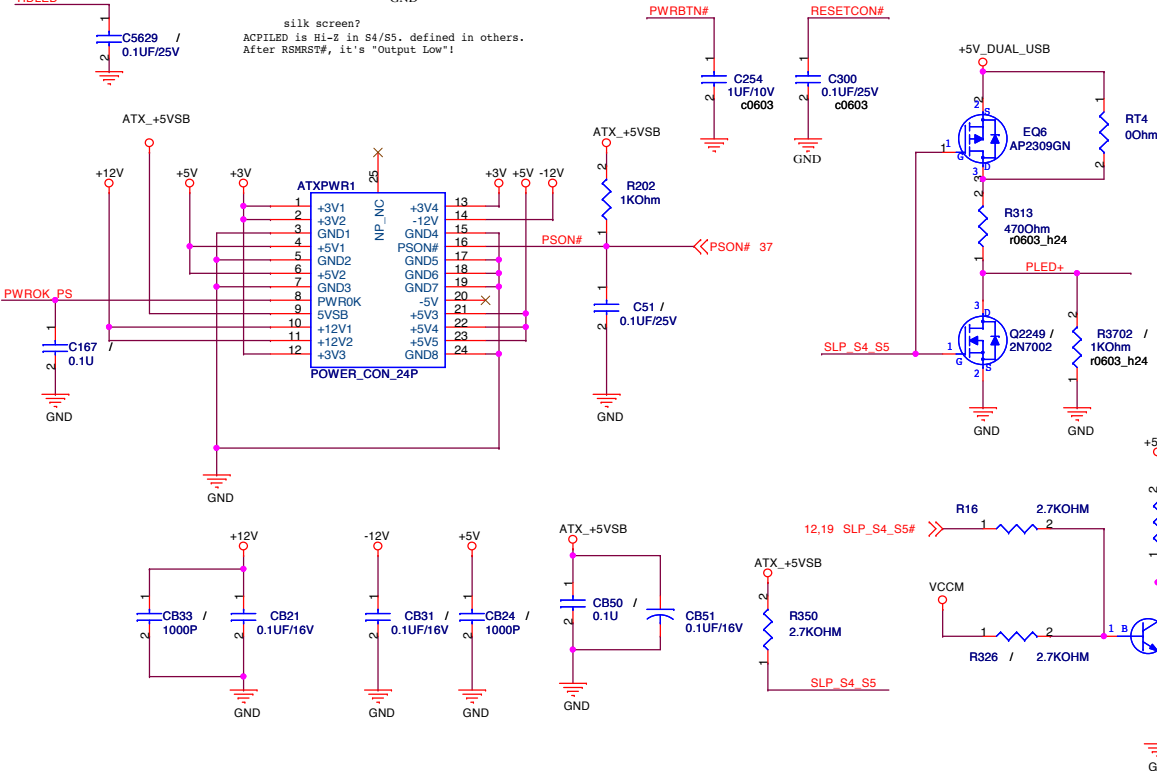
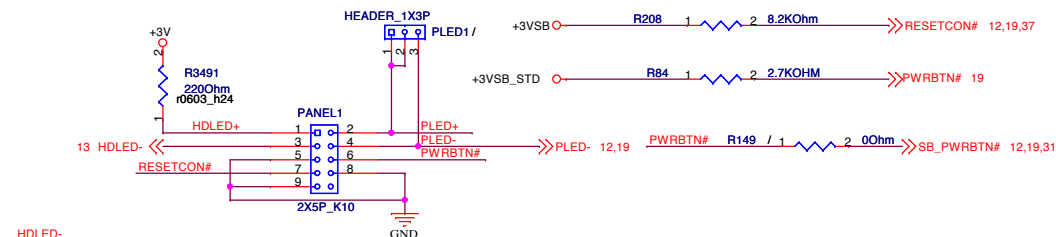
## Speak



## S3



## FRONT PANEL



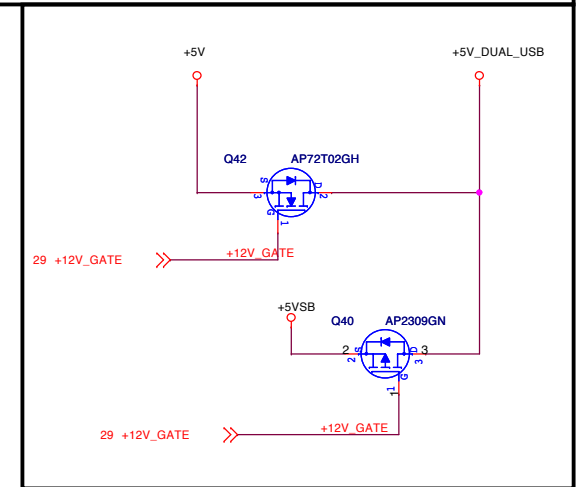
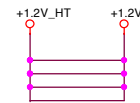
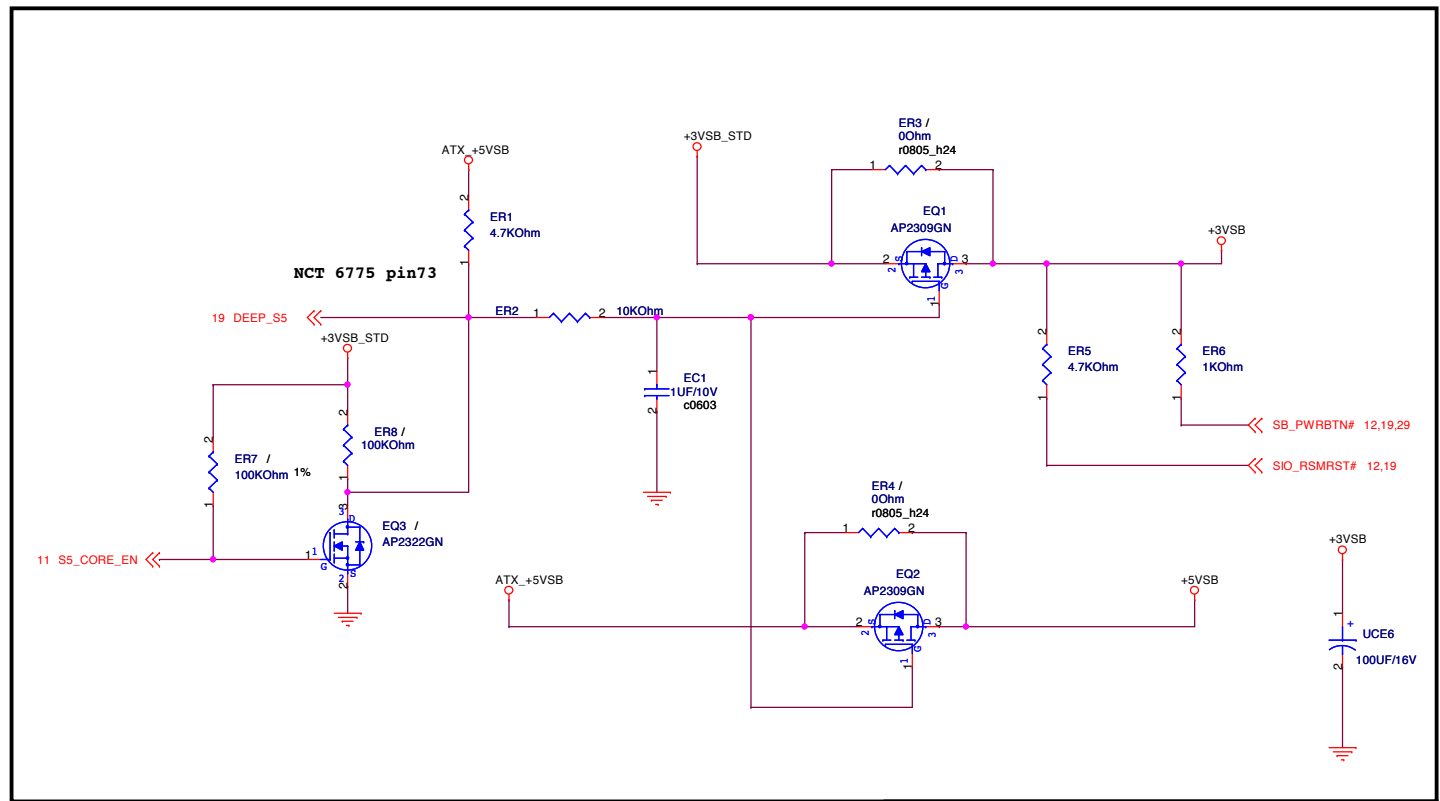
Around the ATX Power Connector

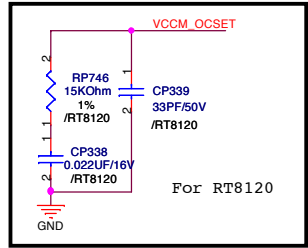
www.vinafix.vn

<Variant Name>

<b>ASRock</b>		Title : POK_DUALSW	
ASRock Inc.		Engineer: Mingus_Wu	
Size	Project Name	A55M-HVS	
A3		Rev 1.03	
Date: Friday, July 22, 2011		Sheet 29	of 39

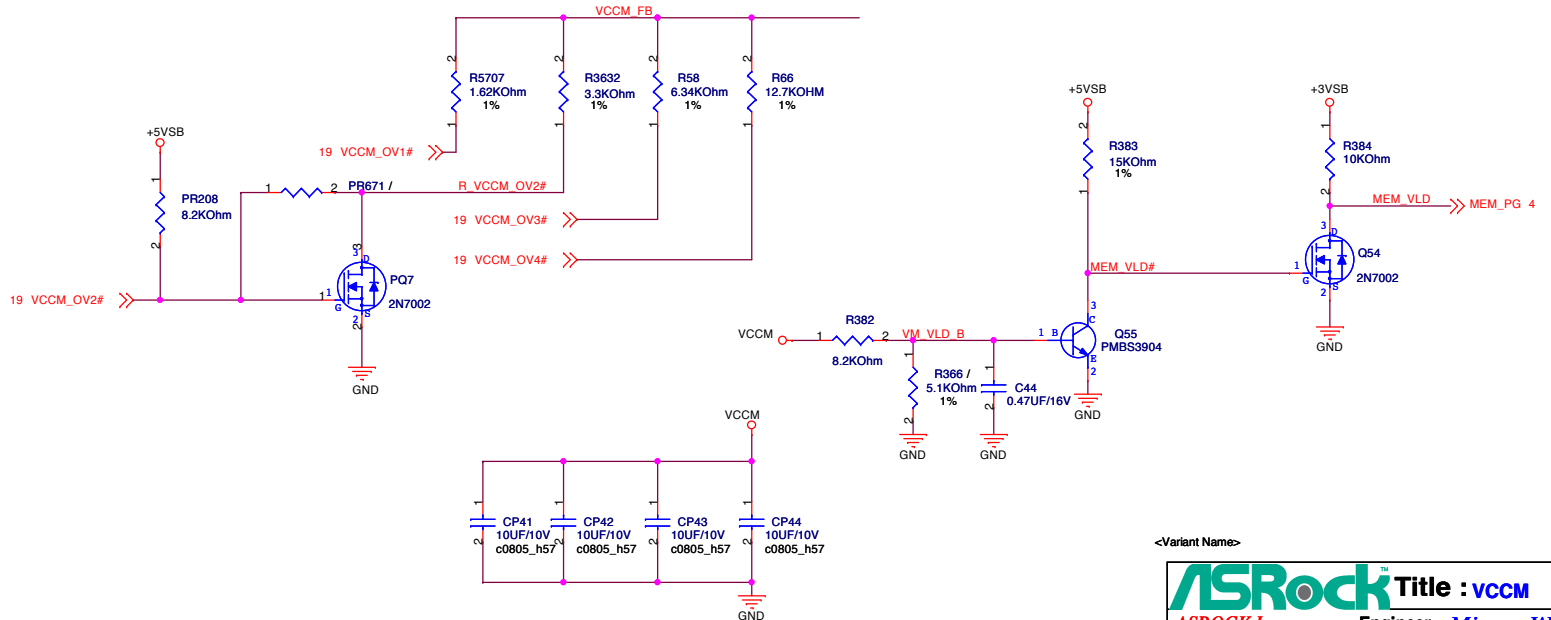






(Power-On default 1.5V )

OV4#	OV3#	OV2#	OV1#	Voltage
I	I	L	I	1.300
L	I	L	I	1.350
I	L	L	I	1.400
L	L	L	I	1.450
I	I	I	I	1.500
L	I	I	I	1.550
I	L	I	I	1.600
L	L	I	I	1.650
I	I	L	L	1.700
L	I	L	L	1.750
I	L	L	L	1.800
L	L	L	L	1.850
I	I	I	L	1.900
L	I	I	L	1.950
I	L	I	L	2.000
L	L	I	L	2.050



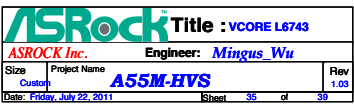
www.vinafix.vn

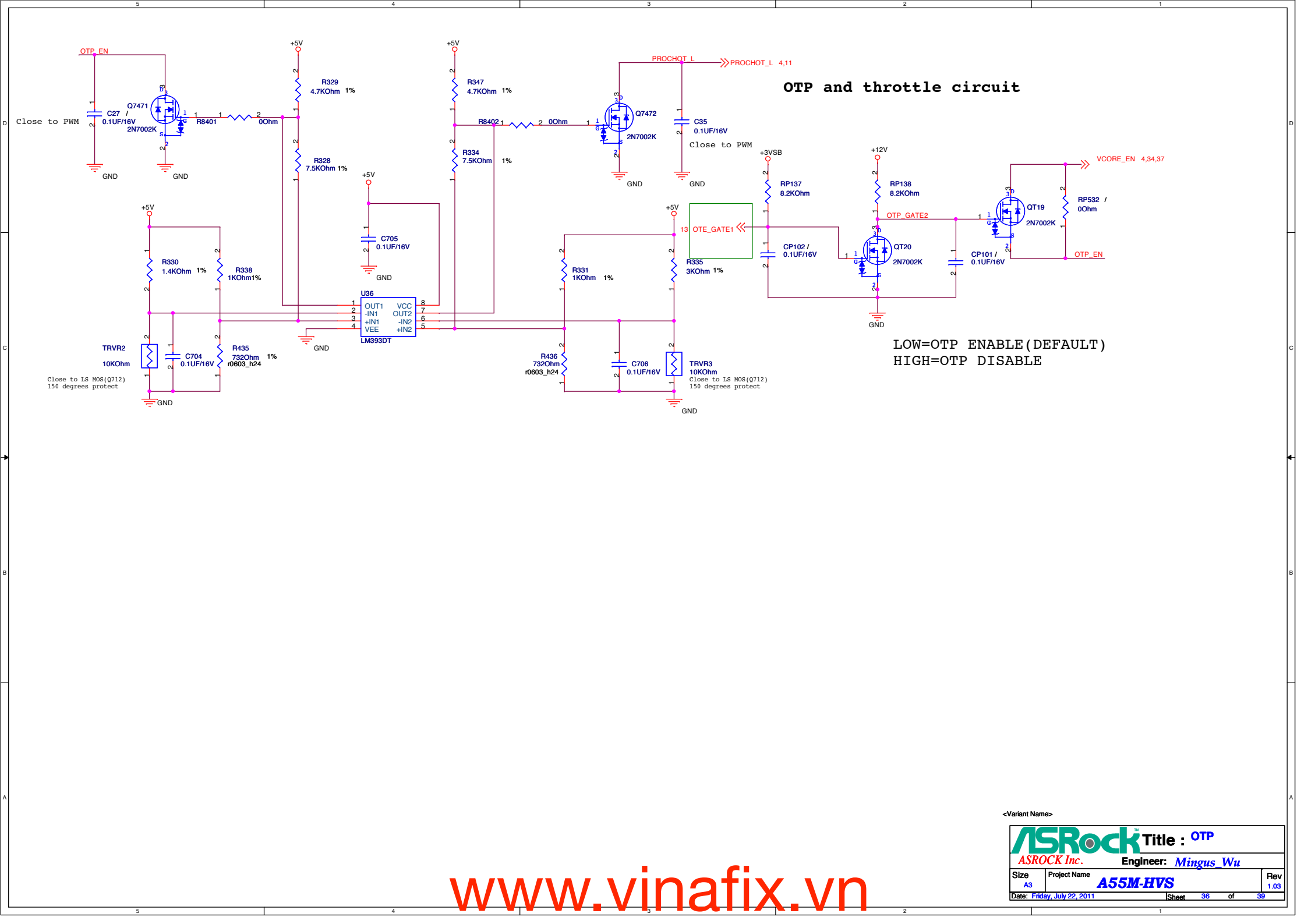
<Variant Name>

		Title : VCCM	
		Engineer: Mingus Wu	
Size	Project Name		Rev
A3	A55M-HVS		
Date: Friday, July 22, 2011	Sheet	32	of 39





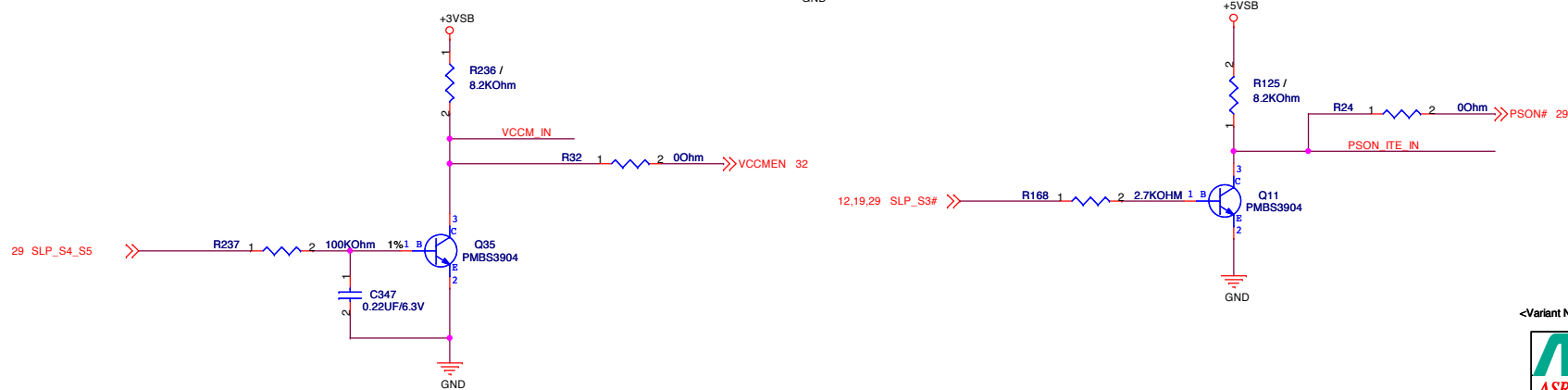
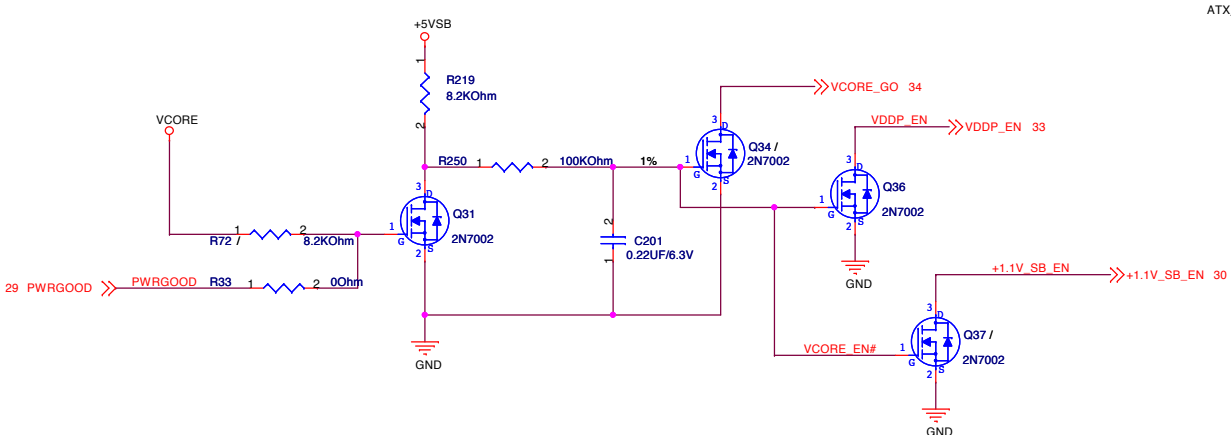
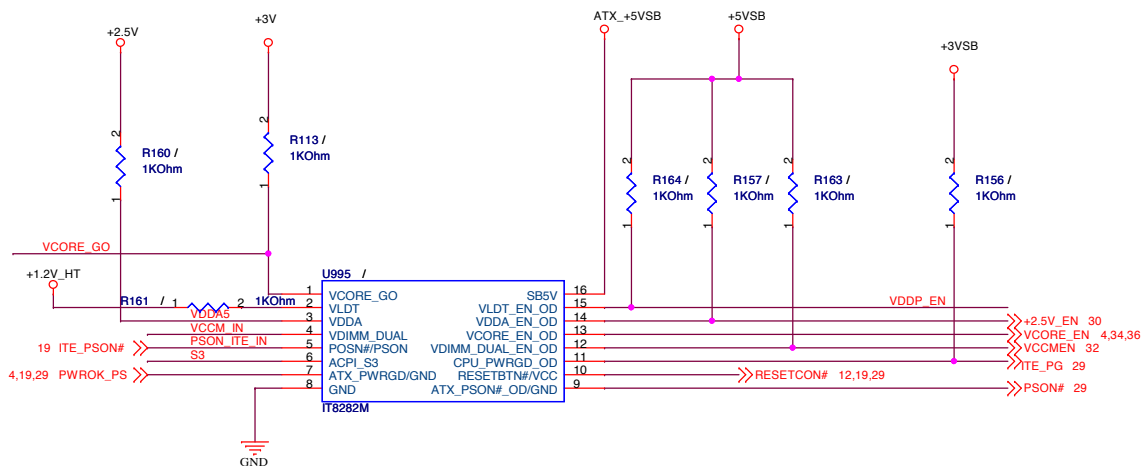




OTP and throttle circuit

LOW=OTP ENABLE (DEFAULT)  
HIGH=OTP DISABLE



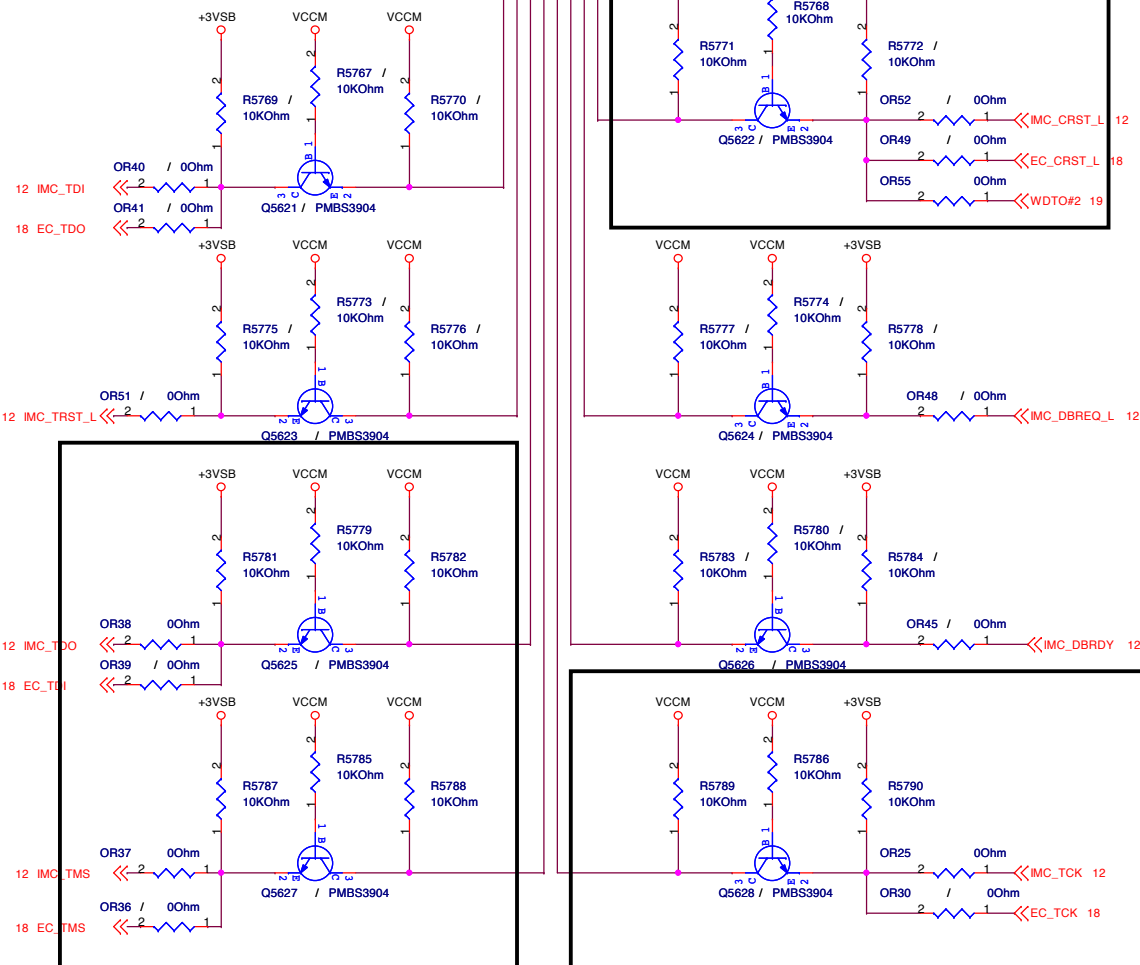


<Variant Name>

		Title : <b>IT8282</b>	
<b>ASROCK Inc.</b>		Engineer: <b>Mingus_Wu</b>	
Size	Project Name		Rev
<b>A3</b>	<b>A55M-HVS</b>		<b>1.03</b>
Date:	Friday, July 22, 2011	Sheet	37 of 39

www.vinafix.vn

4,11 APU\_RST#  
4 CPU\_DBREQ\_L  
4 CPU\_DBRDY  
4 CPU\_TCK  
4 CPU\_TMS  
4 CPU\_TDI  
4 CPU\_TRST\_L  
4 CPU\_TDO

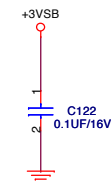
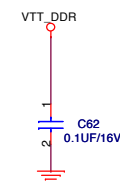
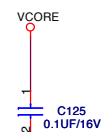
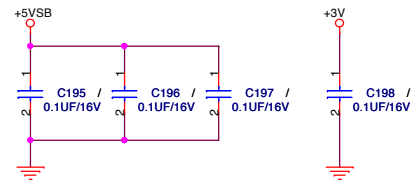
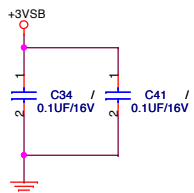
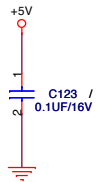
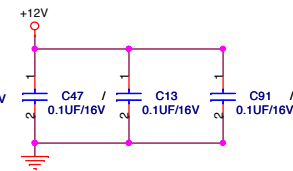
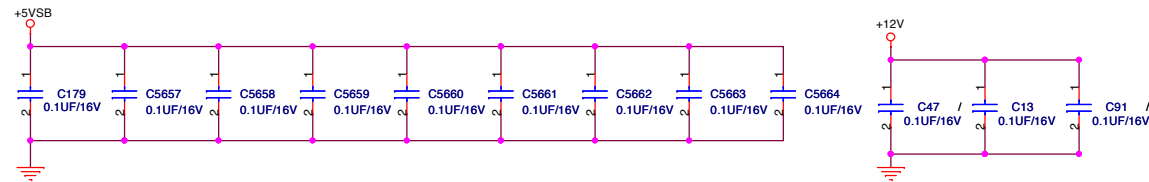
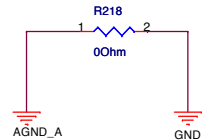
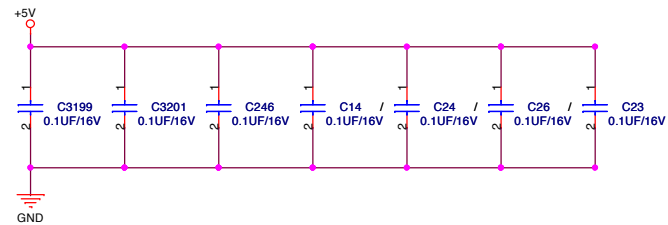
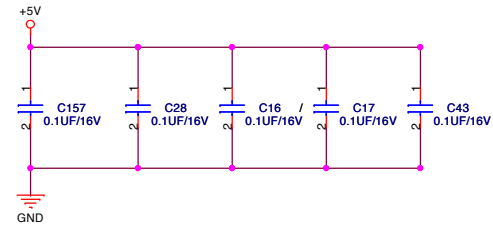
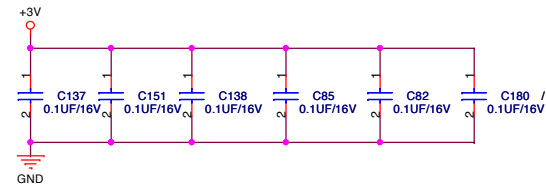
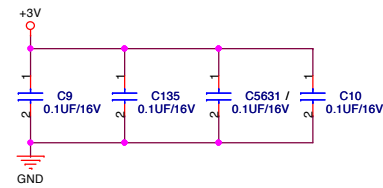
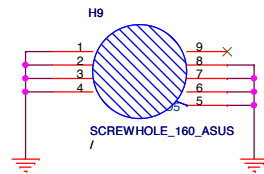
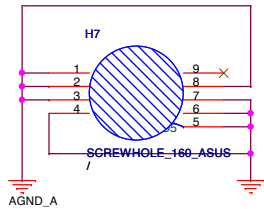
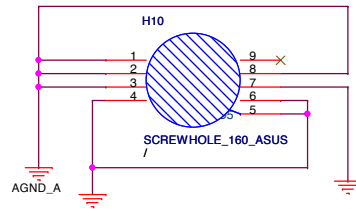
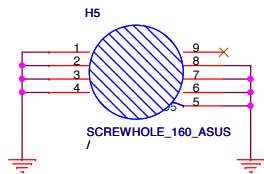
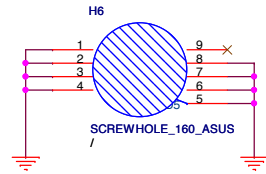
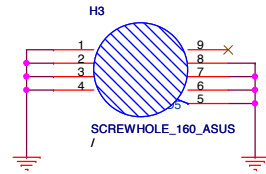


www.vinafix.vn

<Variant Name>

ASRock Inc.		Title : ACC & EUP & IOT
ASRock Inc.		Engineer: Mingus Wu
Size A3	Project Name A55M-HVS	Rev 1.03
Date: Friday, July 22, 2011		Sheet 38 of 39

# uATX scew



www.vinafix.vn

<Variant Name>

ASRock		Title : SCREW	
ASRock Inc.		Engineer: Mingus_Wu	
Size	A3	Project Name	A55M-HVS
Date	Friday, July 22, 2011	Sheet	39 of 39
Rev	1.03		